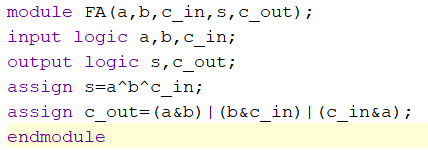
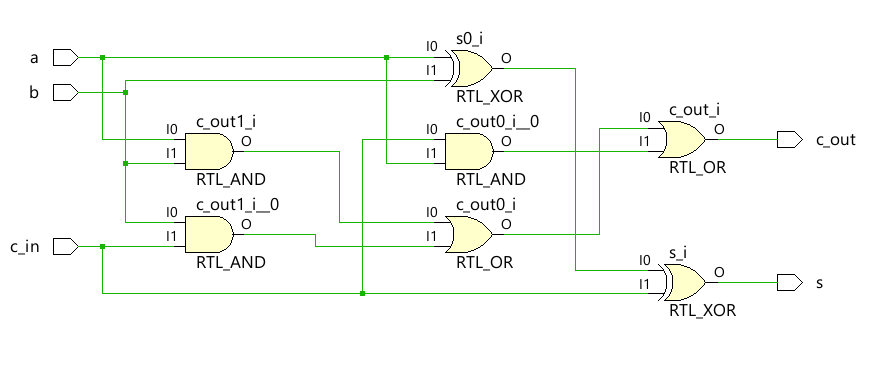
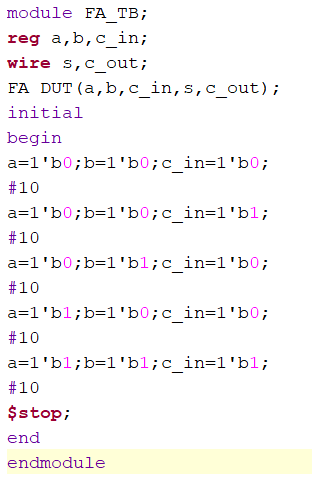
# CADD RECORD

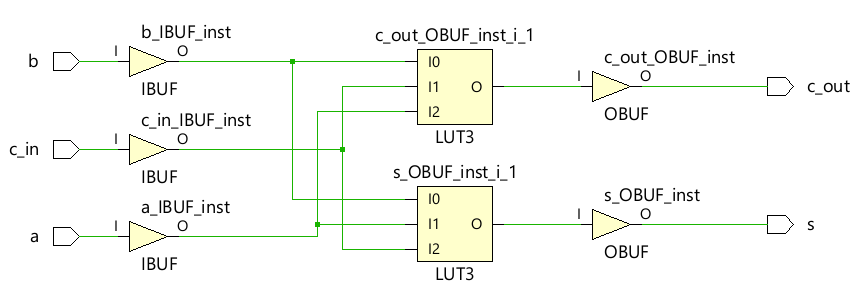
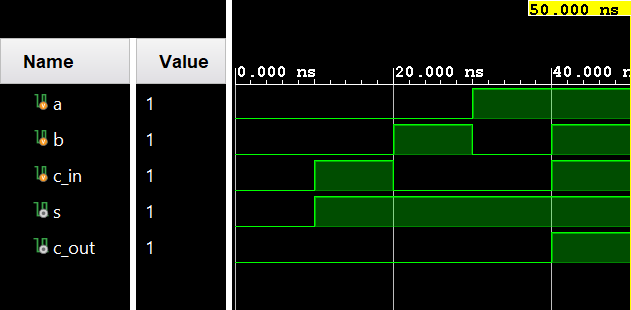
**SRN:** PES2UG23EC027 **NAME:** Arpan Royston Cutinha

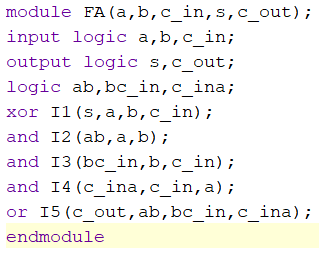
**CLASS:** 3 ‘A’

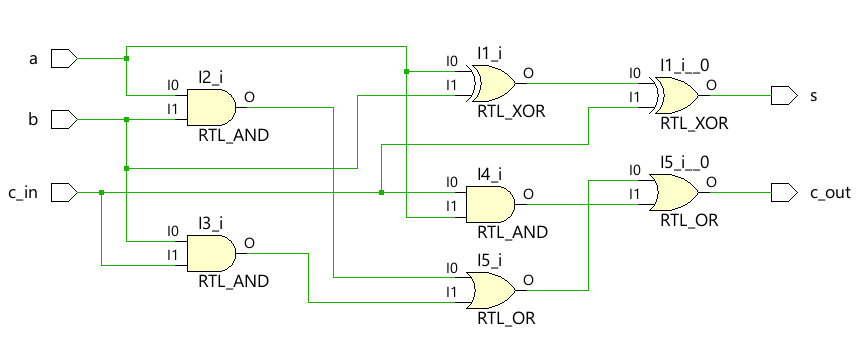
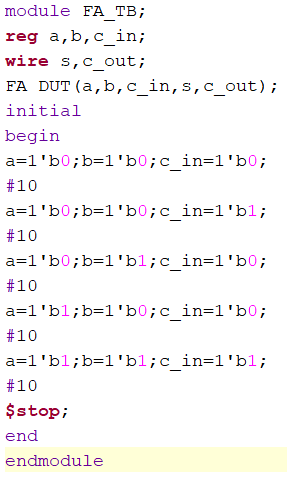
**INDEX :**

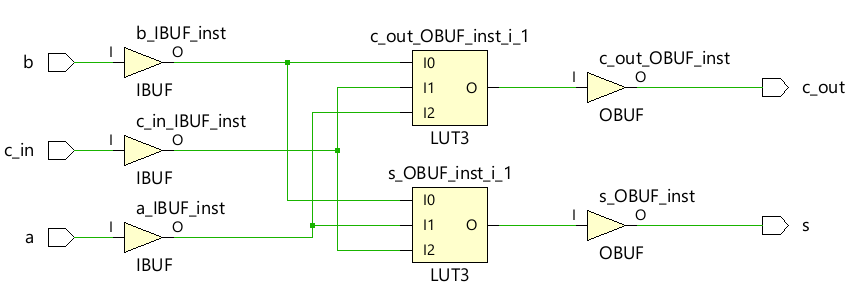
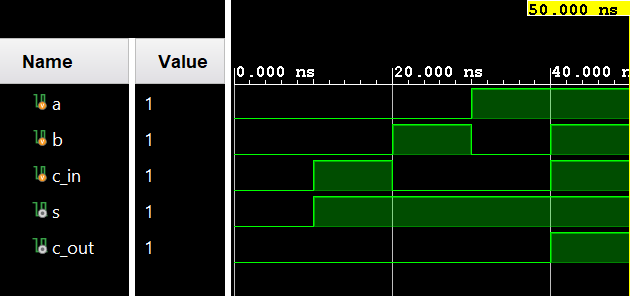
1. **Full Adder (Dataflow Style)**
2. **Full Adder – Structural Style**
3. **Full Adder – Using Two Half Adders (Structural Style)**
4. **Logic Gates (All Gates)**
5. **4:1 Mux – Dataflow Style**
6. **4:1 Mux using 2:1 Mux (Structural Style)**
7. **4:1 Mux Using two level logic (Structural Style)**
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9. **Binary to Gray code converter**
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12. **4-bit Ripple Carry Adder**
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16. **2 to 4 Decoder**
17. **Full Adder using 4:1 Mux**
18. **Tristate Buffer**
19. **Binary Multiplier**
20. **Full Adder with 3 to 8 Decoder**
21. **D - Latch**
22. **SR - Latch**
23. **D - FF**
24. **SR - FF**
25. **UP - Counter**
26. **Full Adder**(Dataflow Style)****

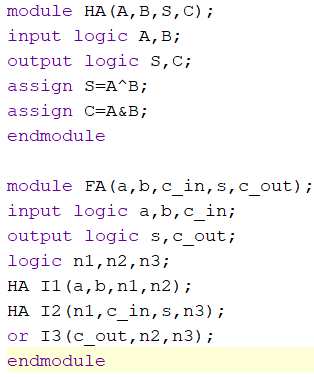
****

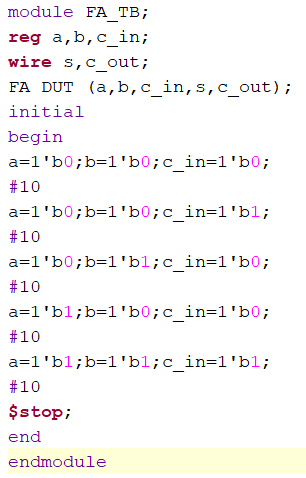


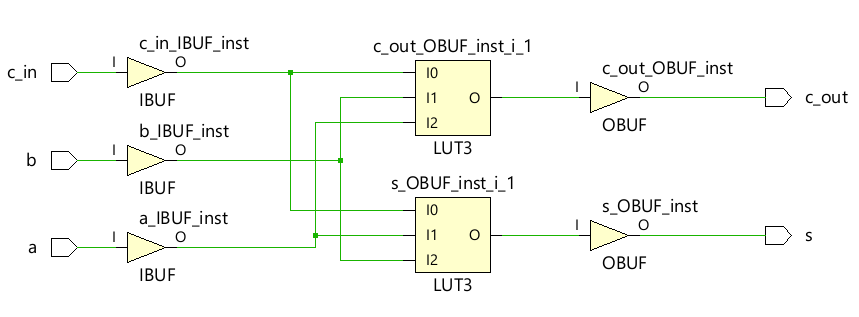
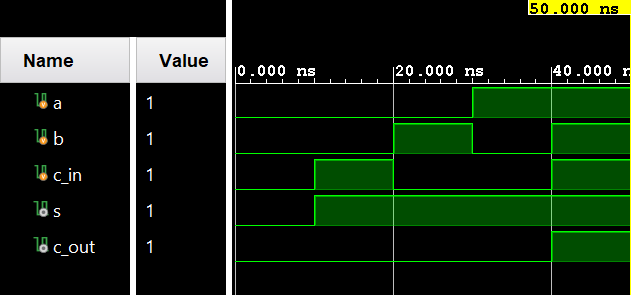
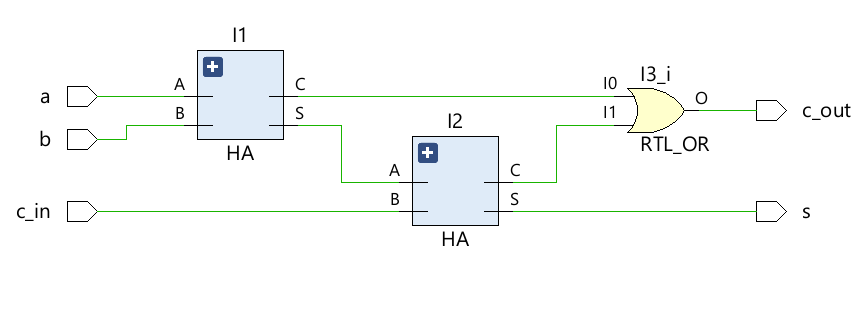
1. **Full Adder**(Structural Style)

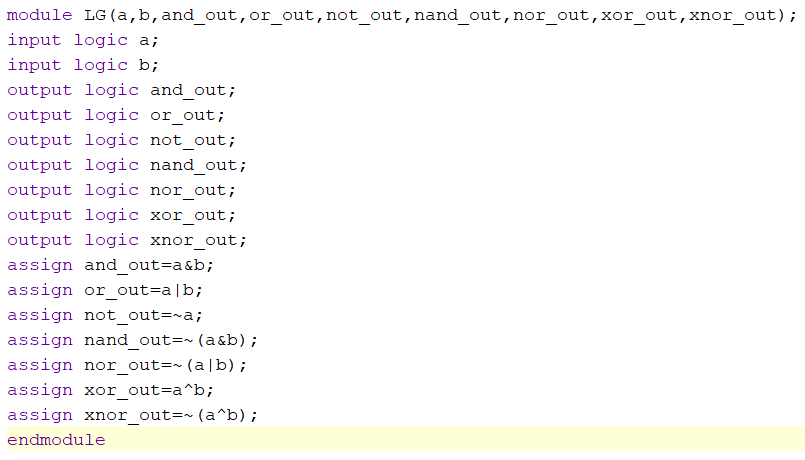
****

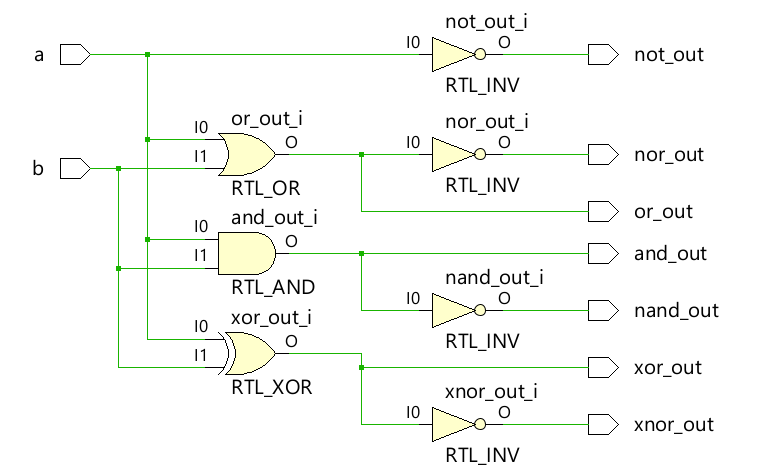
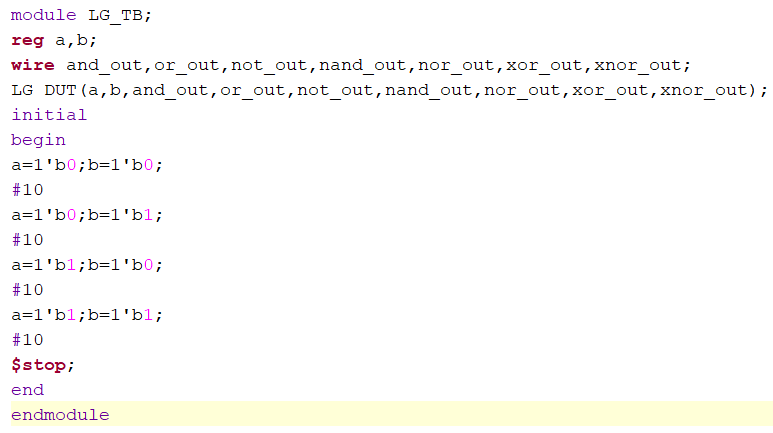


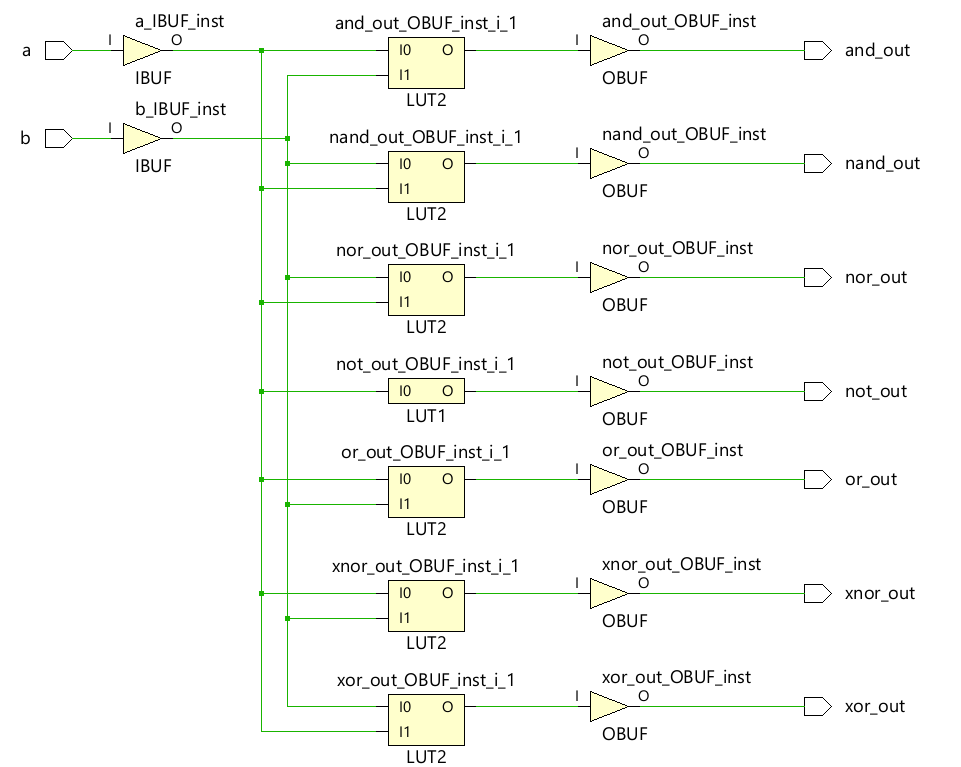
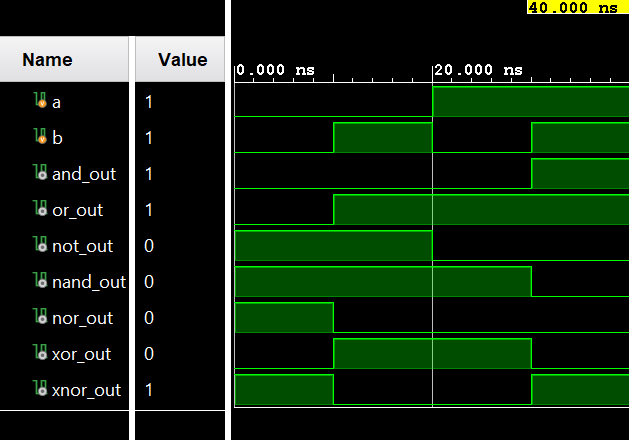
1. **Full Adder –** Using Two Half Adders (Structural Style)

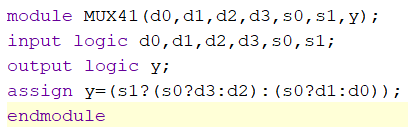


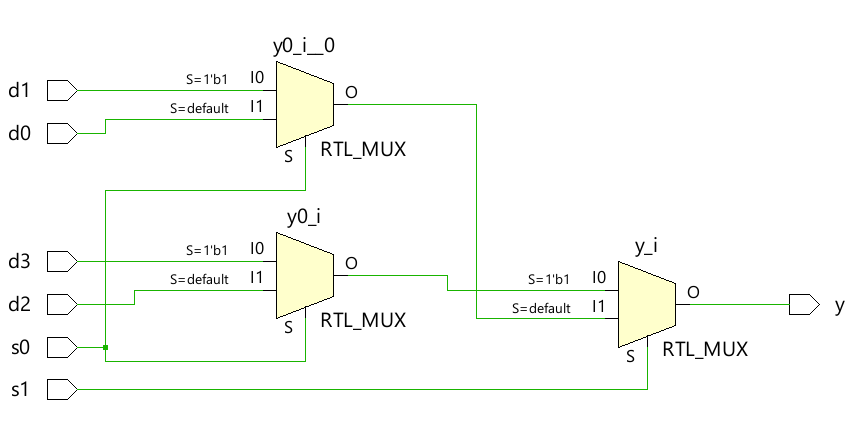
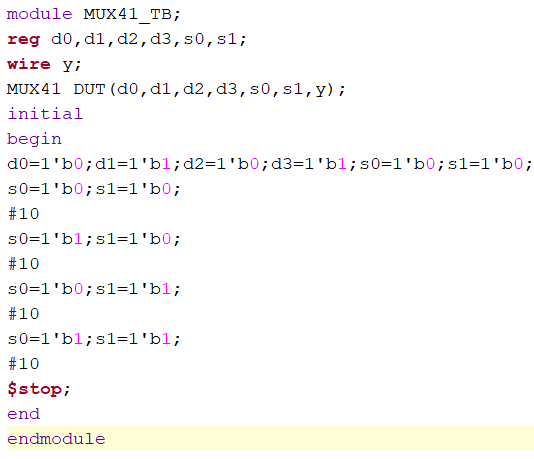


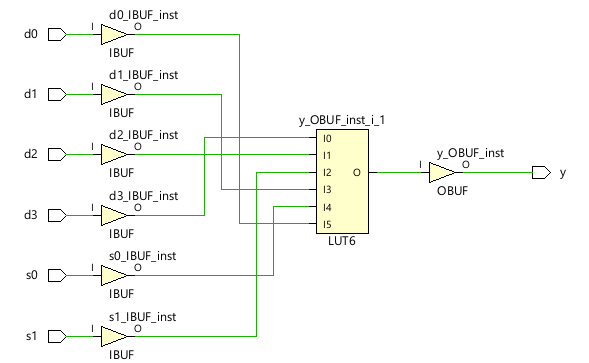
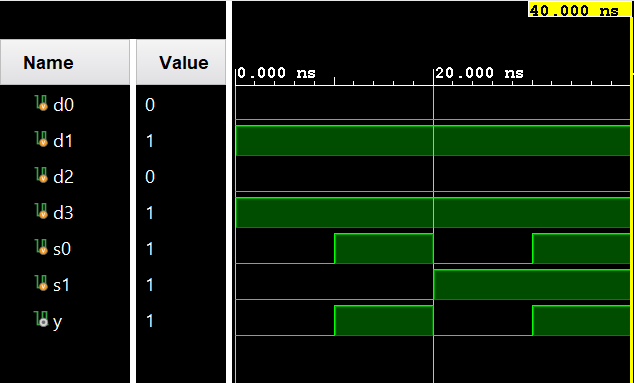
1. **Logic Gates** (All Gates)

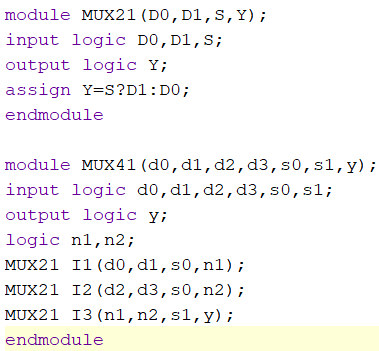


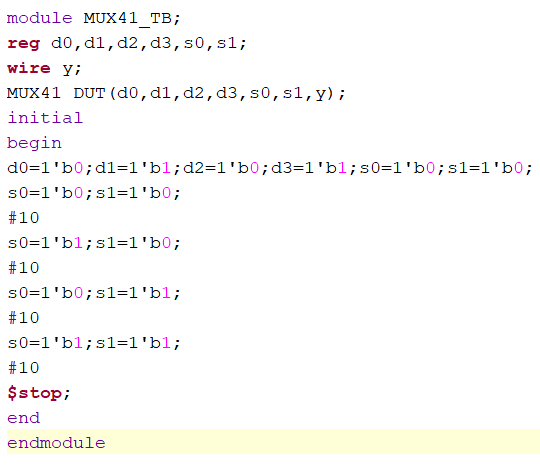


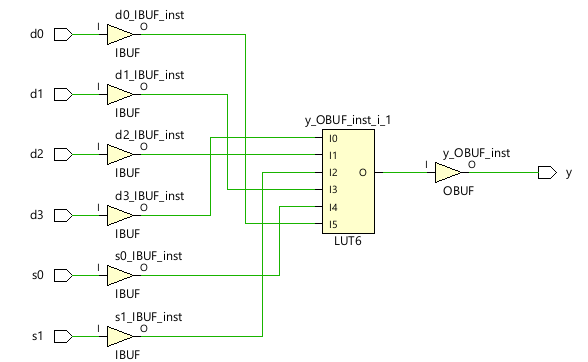
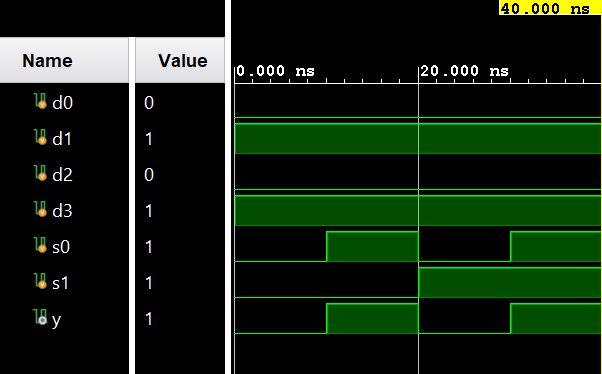
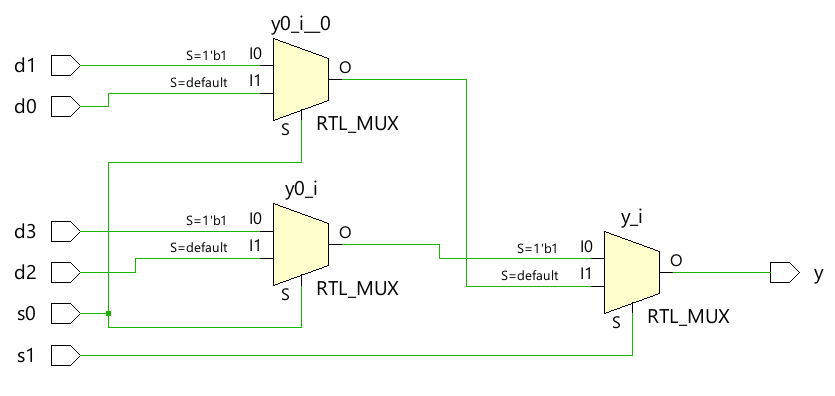
1. **4:1 Mux –** Dataflow Style

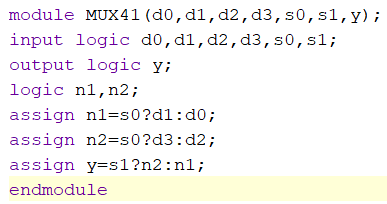


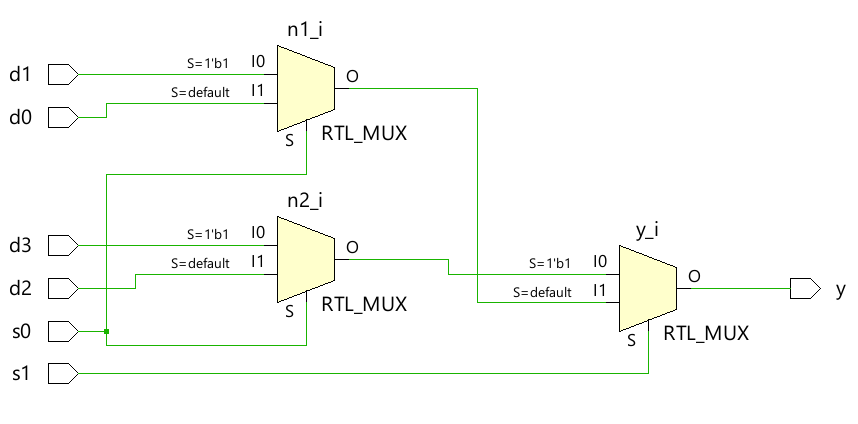
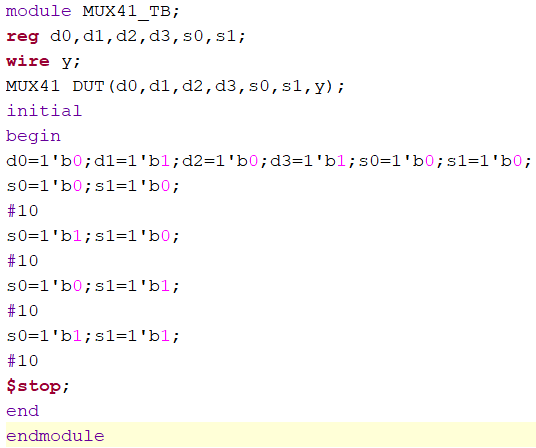


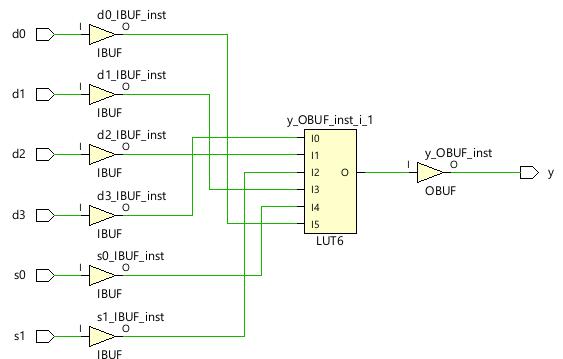
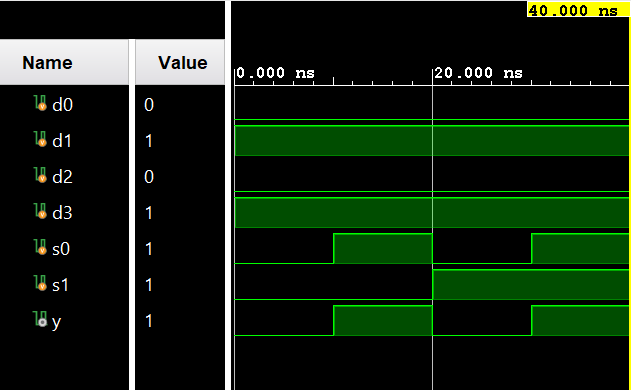
1. **4:1 Mux using 2:1 Mux** (Structural Style)

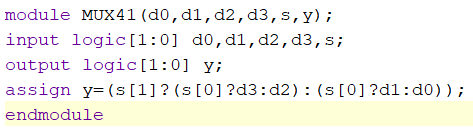


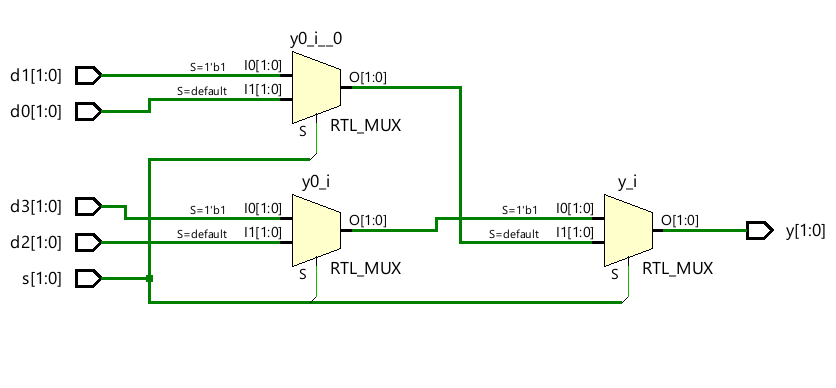
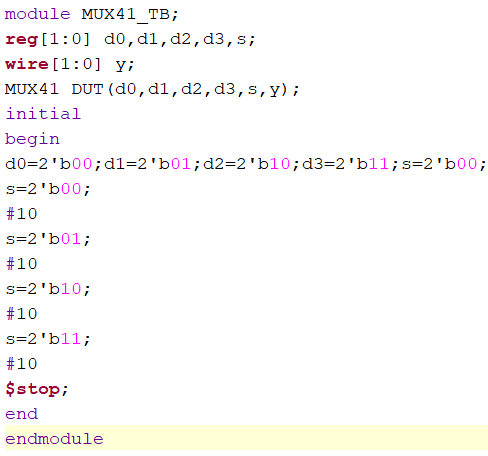


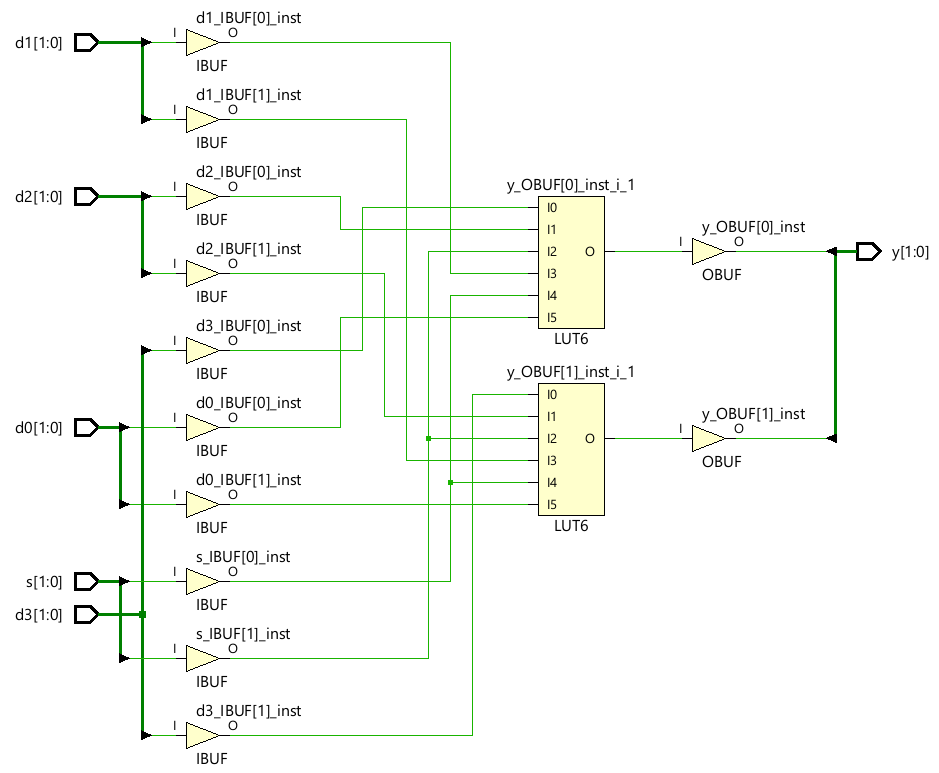
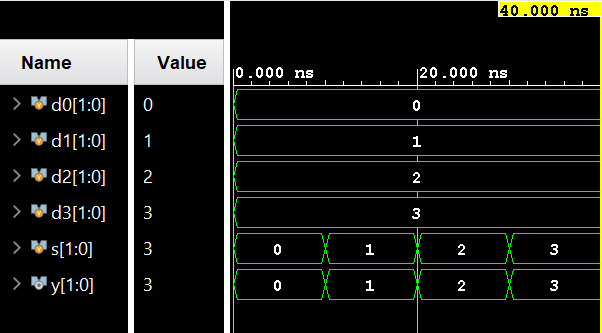
1. **4:1 Mux Using two level logic** (Structural Style)

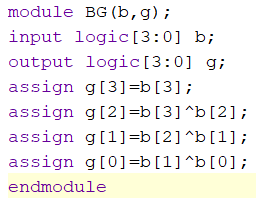
****

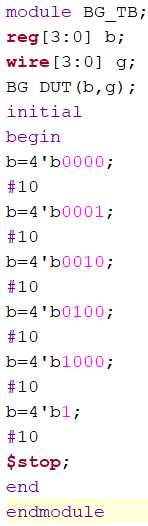


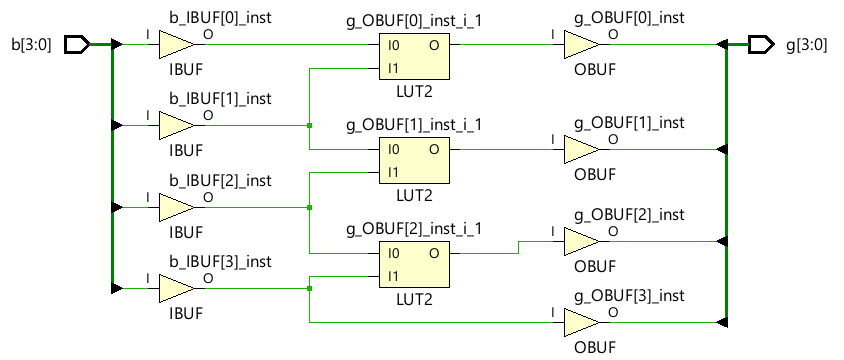
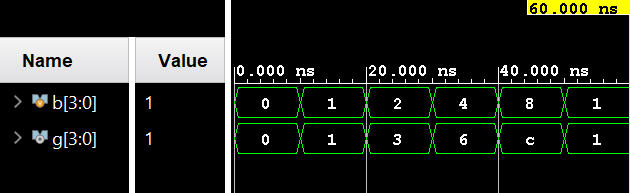
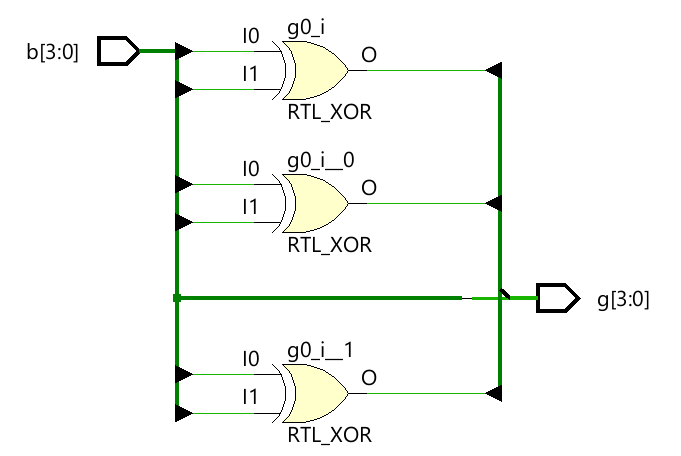
1. **2 bits wide 4:1 Mux –** Dataflow Style

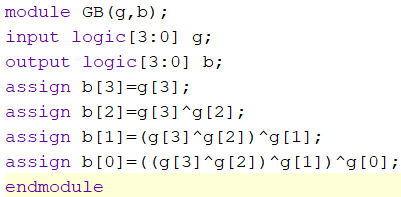
****

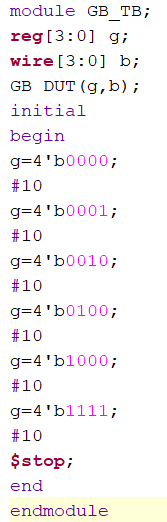


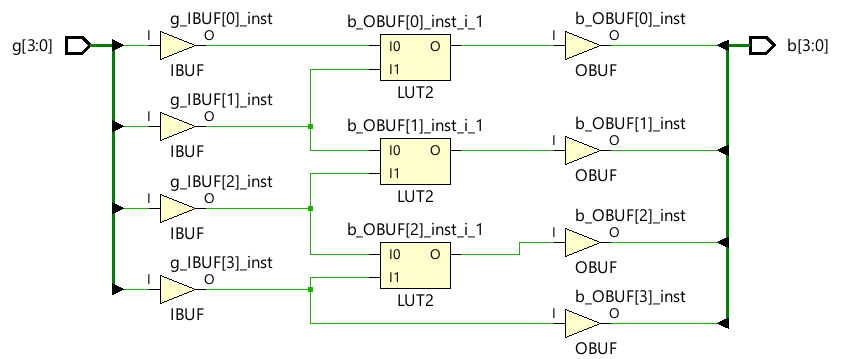
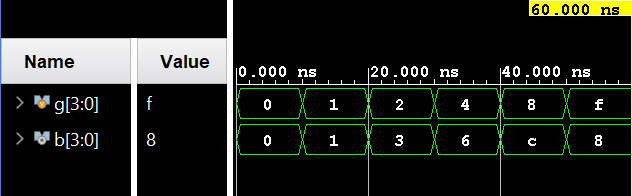
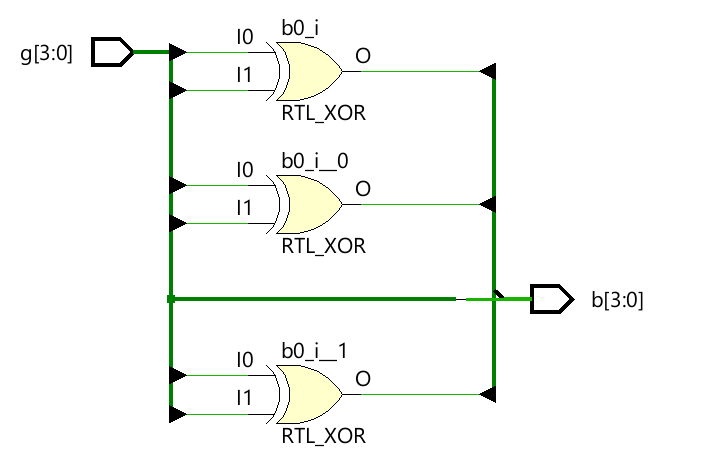
1. **Binary to Gray code converter**

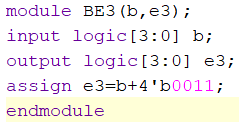
****

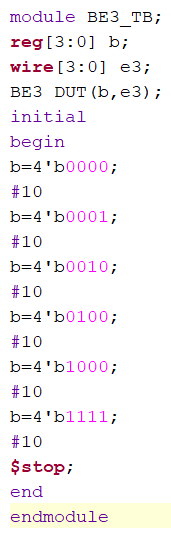
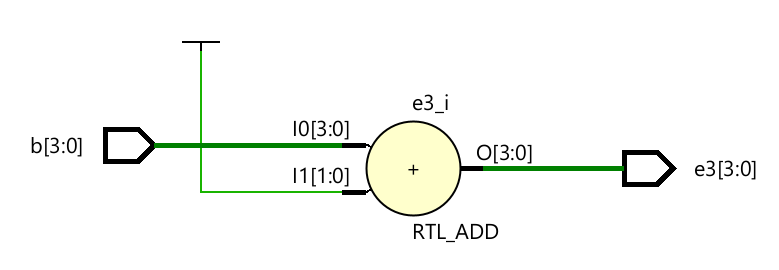


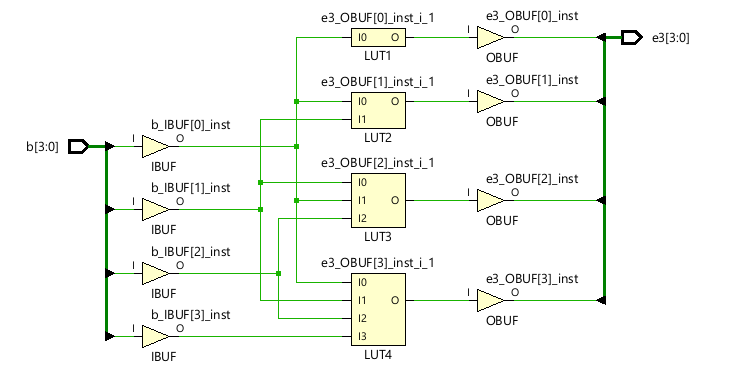
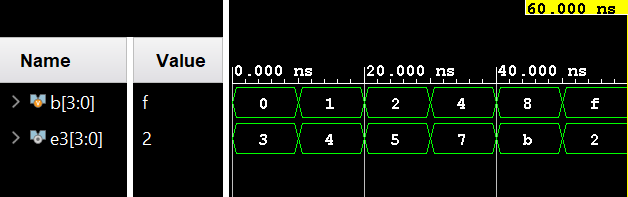
1. **Gary to Binary code converter**

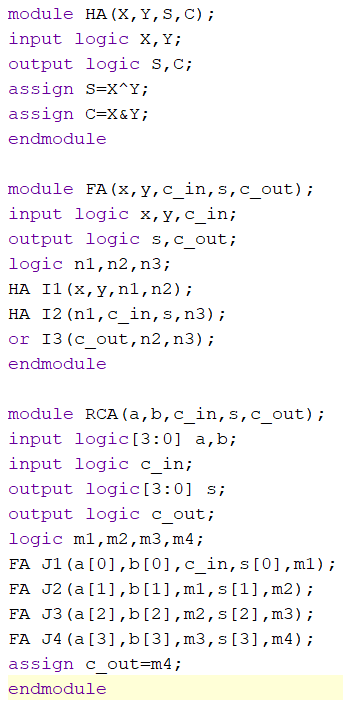
****

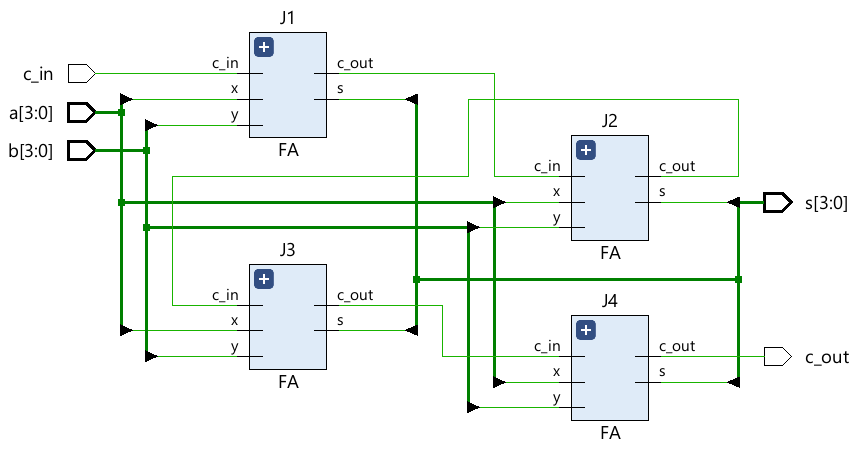
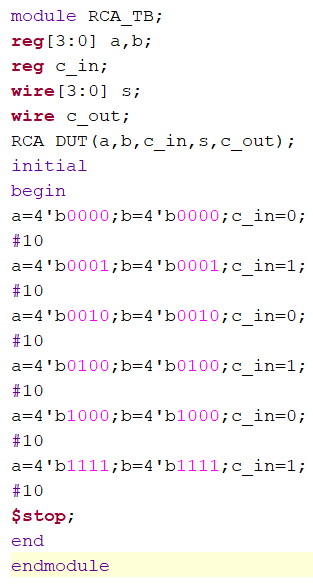


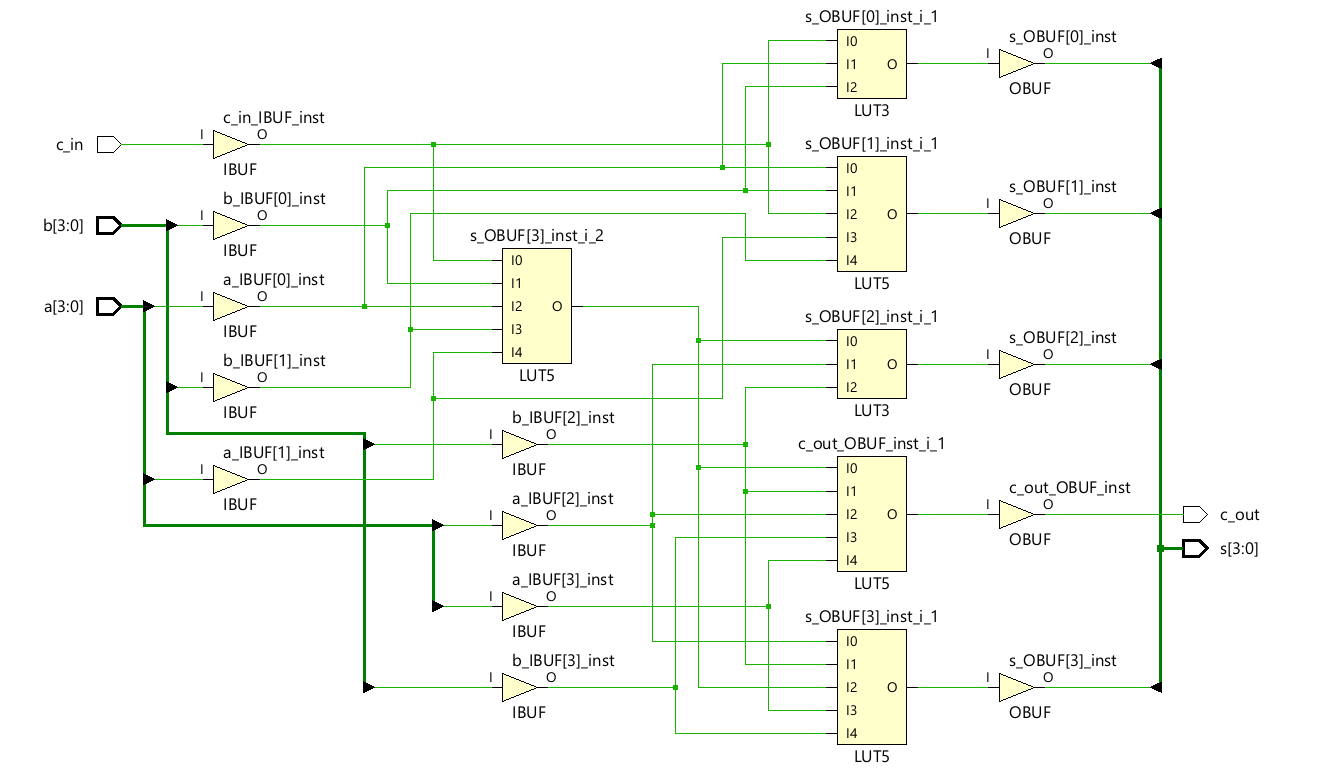
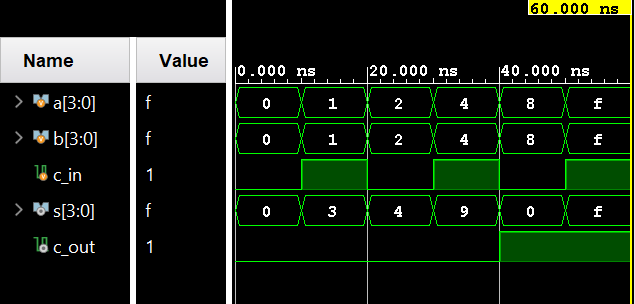
1. **Binary to Excess 3 code converter**

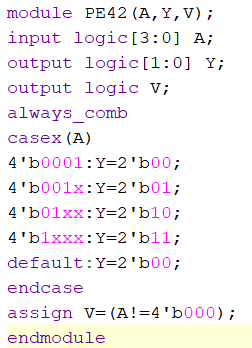
****

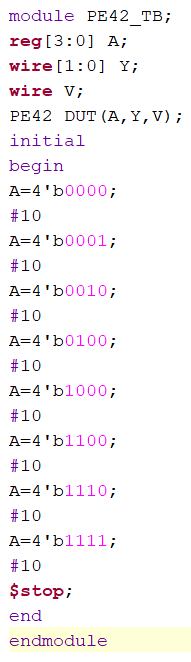


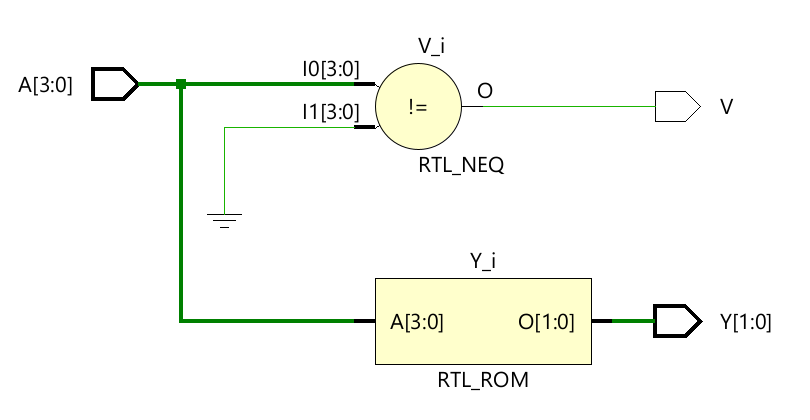
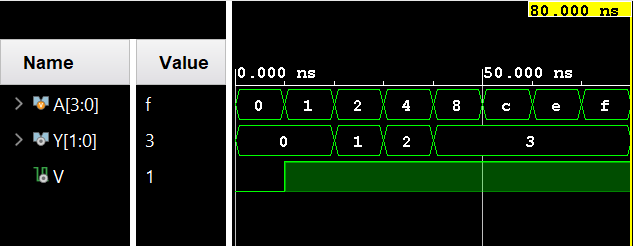
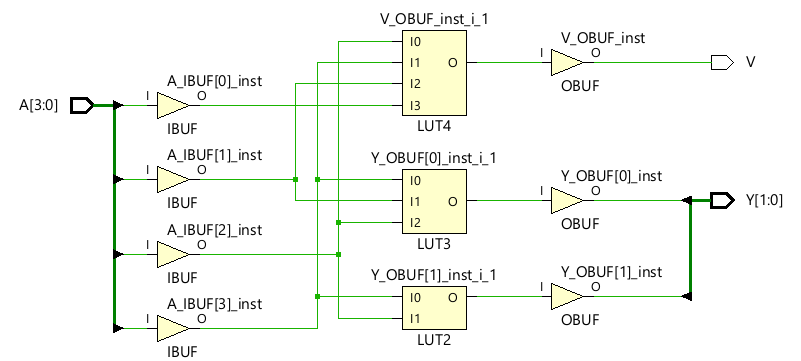
1. **4-bit Ripple Carry Adder**

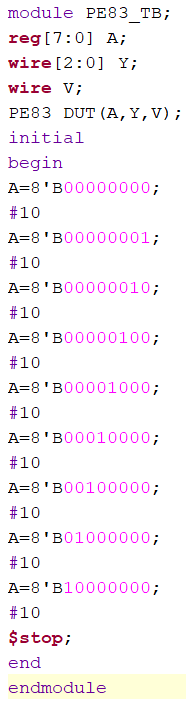
****

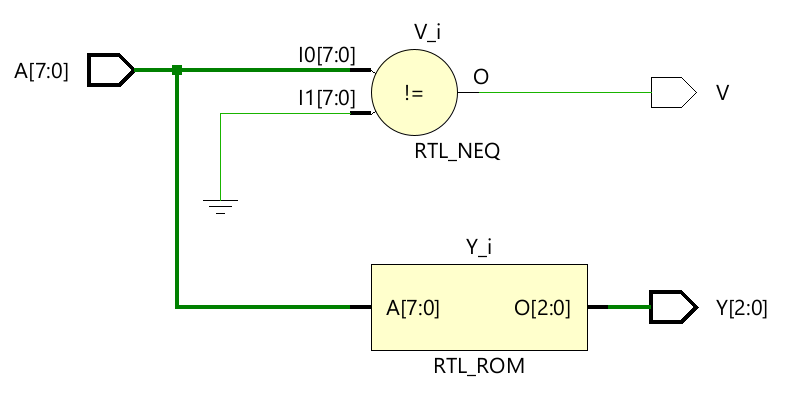
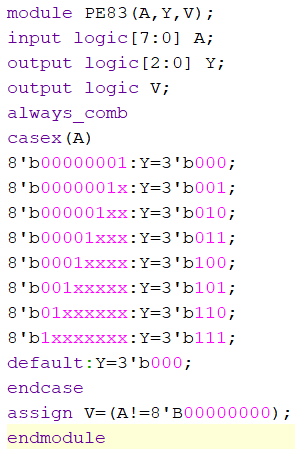


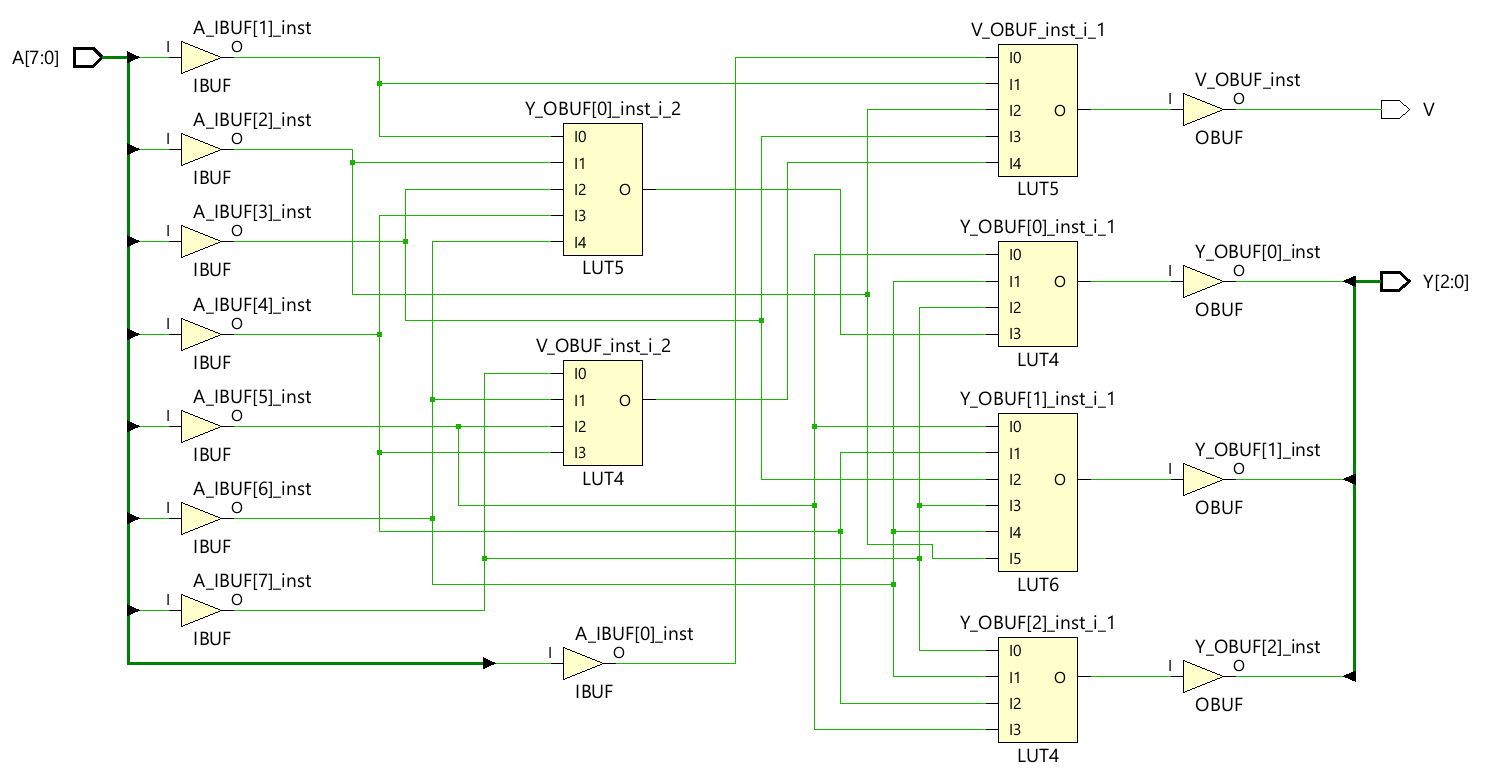
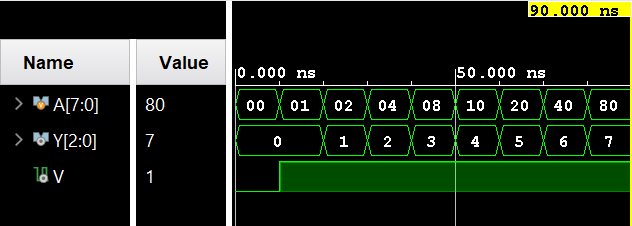
1. **4 to 2 Priority Encoder**

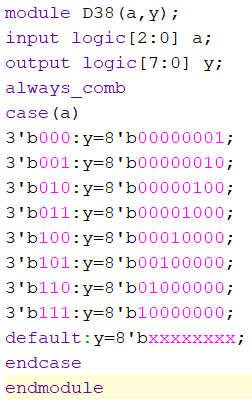
****

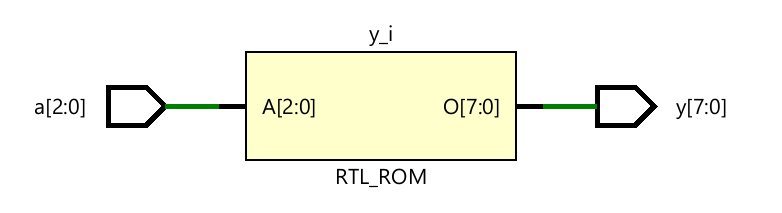
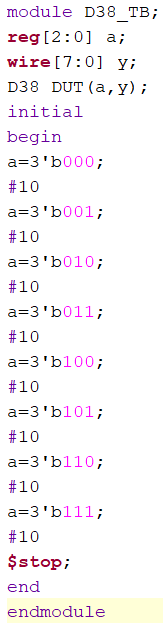


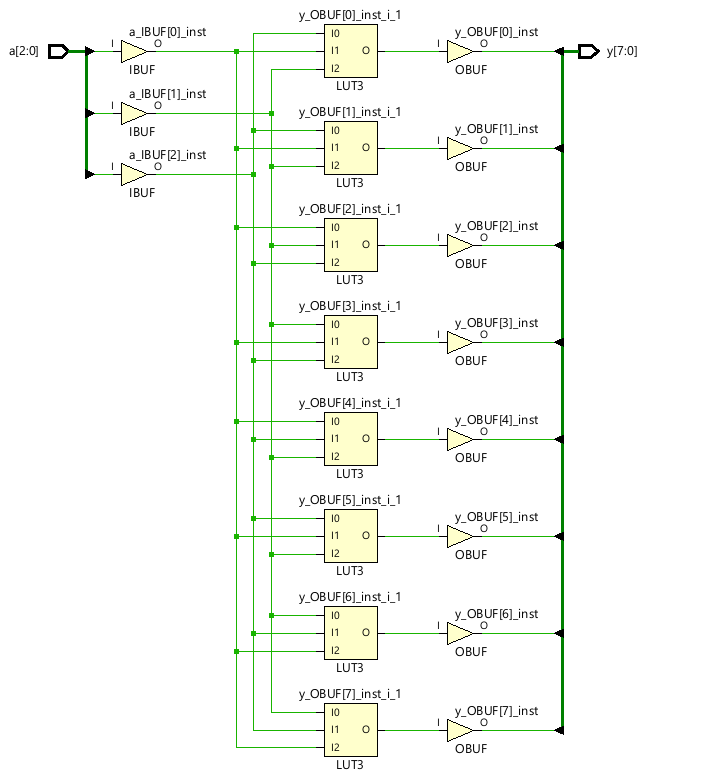
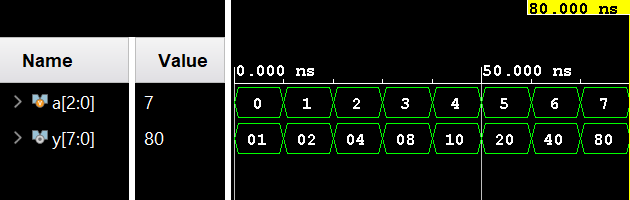
1. **8 to 3 Priority Encoder with a valid bit**

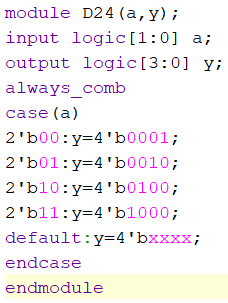
****

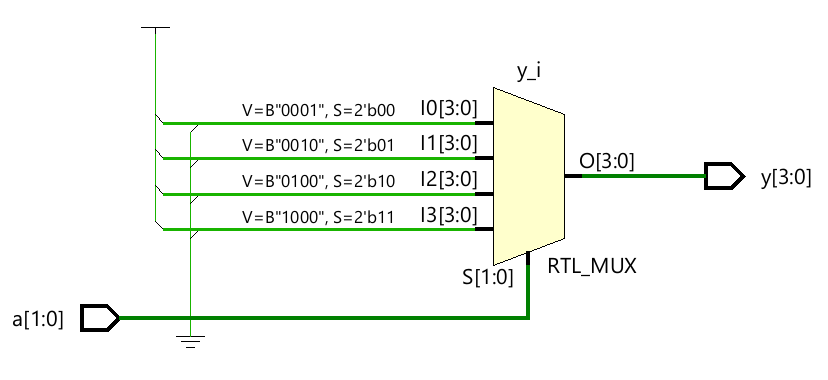
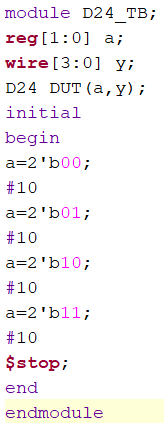
****

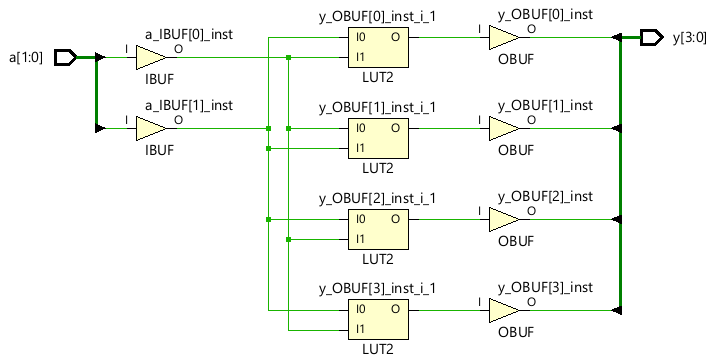
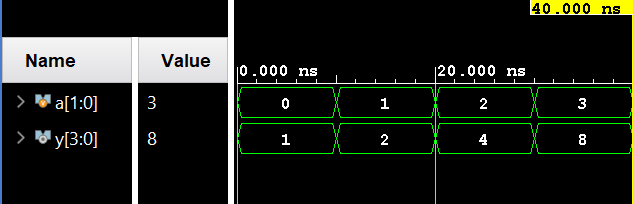
1. **3 to 8 Decoder**

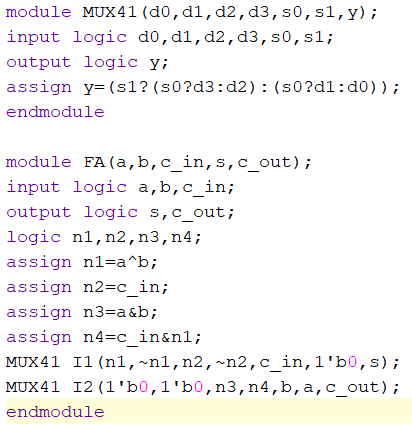
****

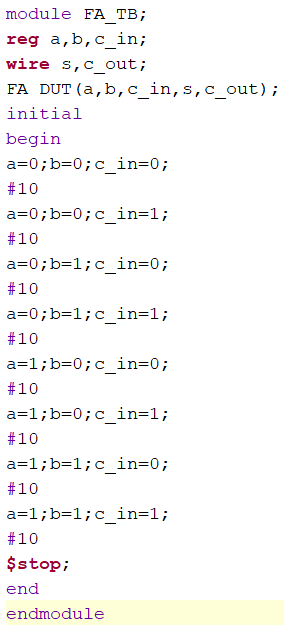
****

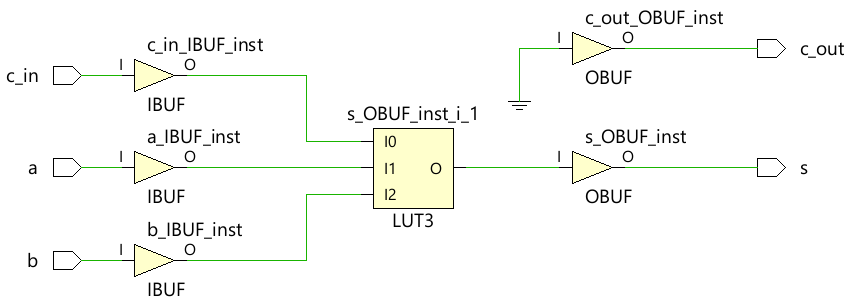
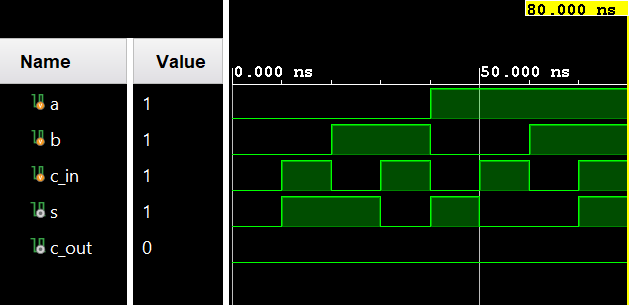
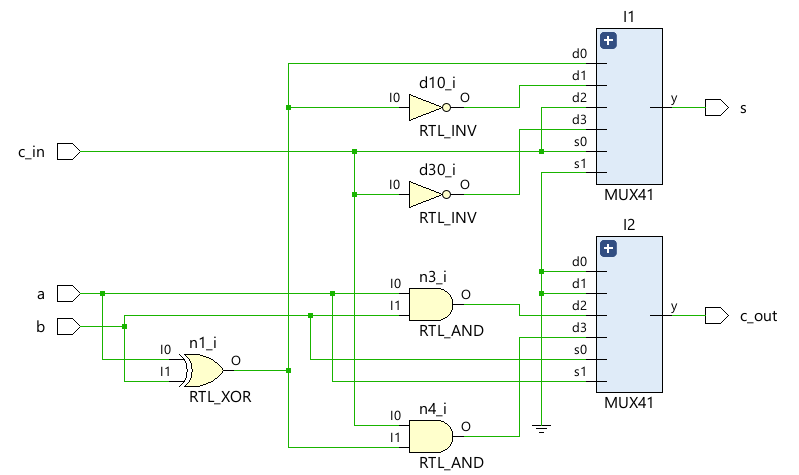
1. **2 to 4 Decoder**

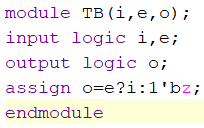
****

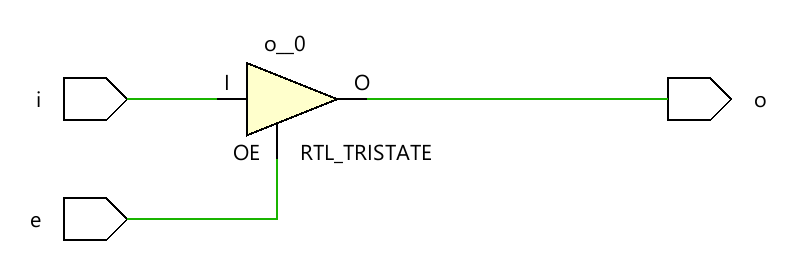
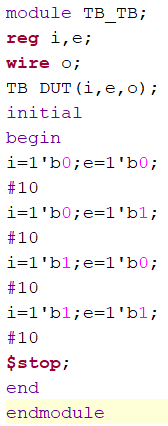
****

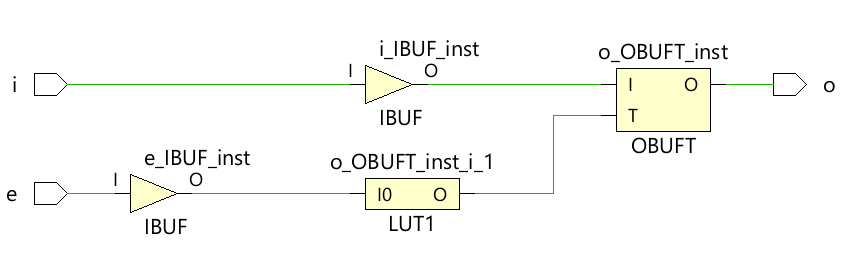
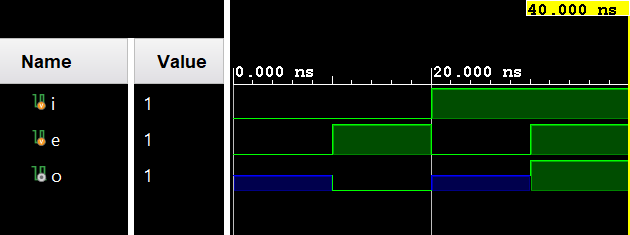
1. **Full Adder using 4:1 Mux**

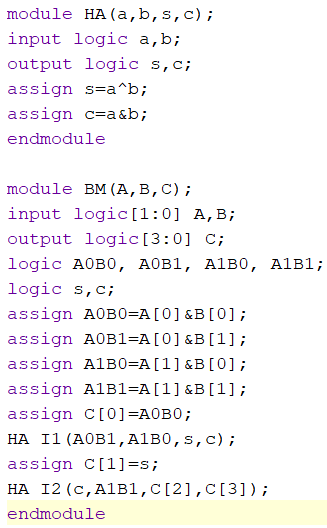
****

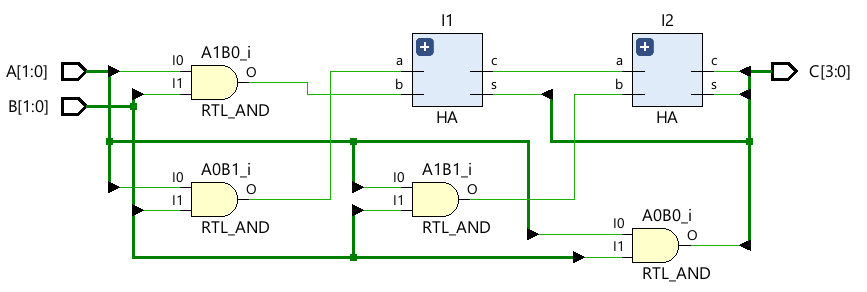
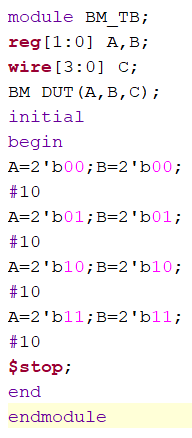
****

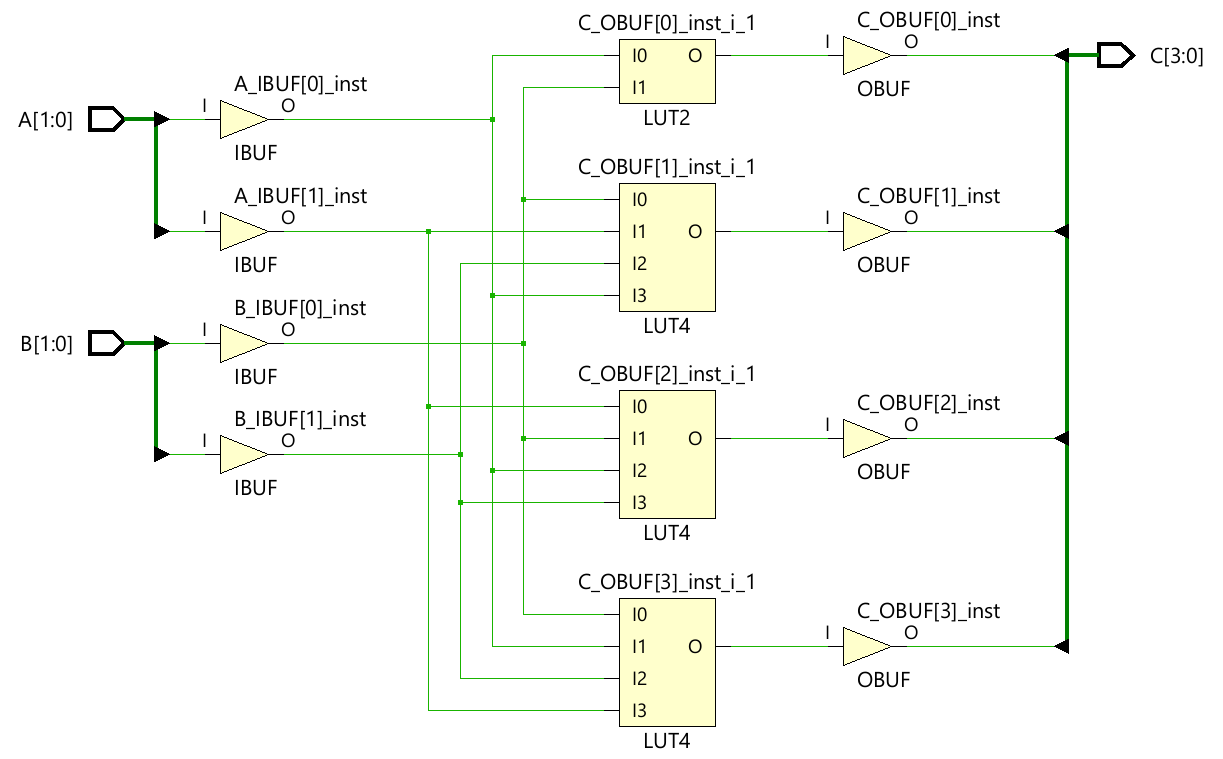
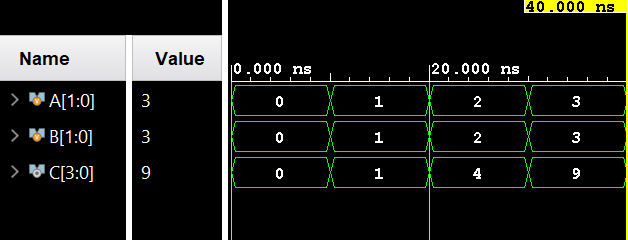
1. **Tristate Buffer**

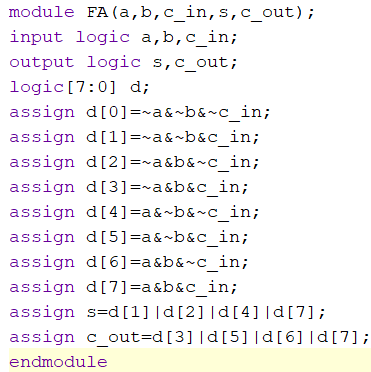
****

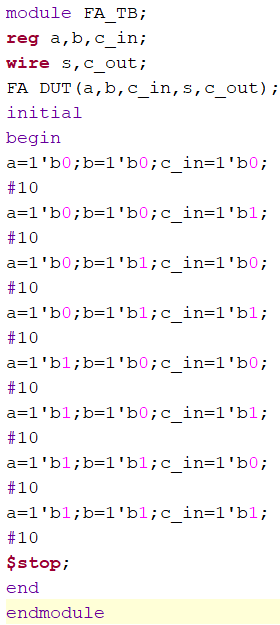
****

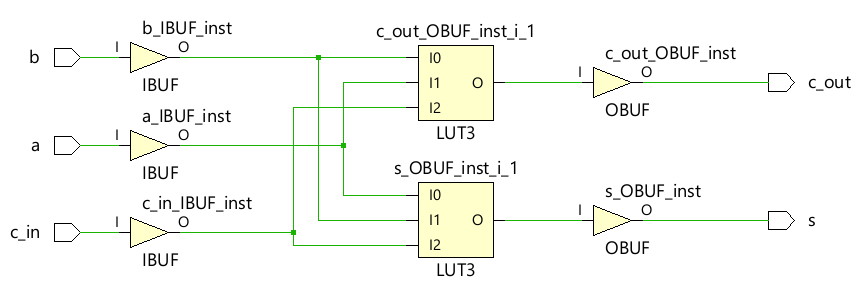
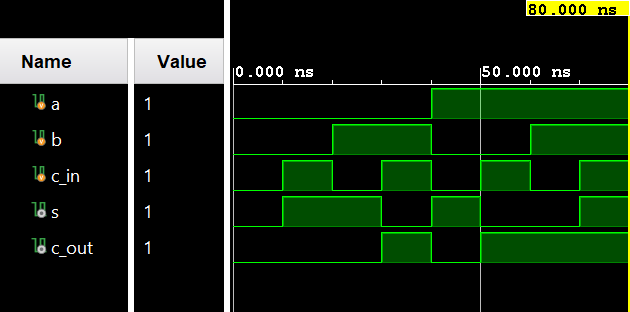
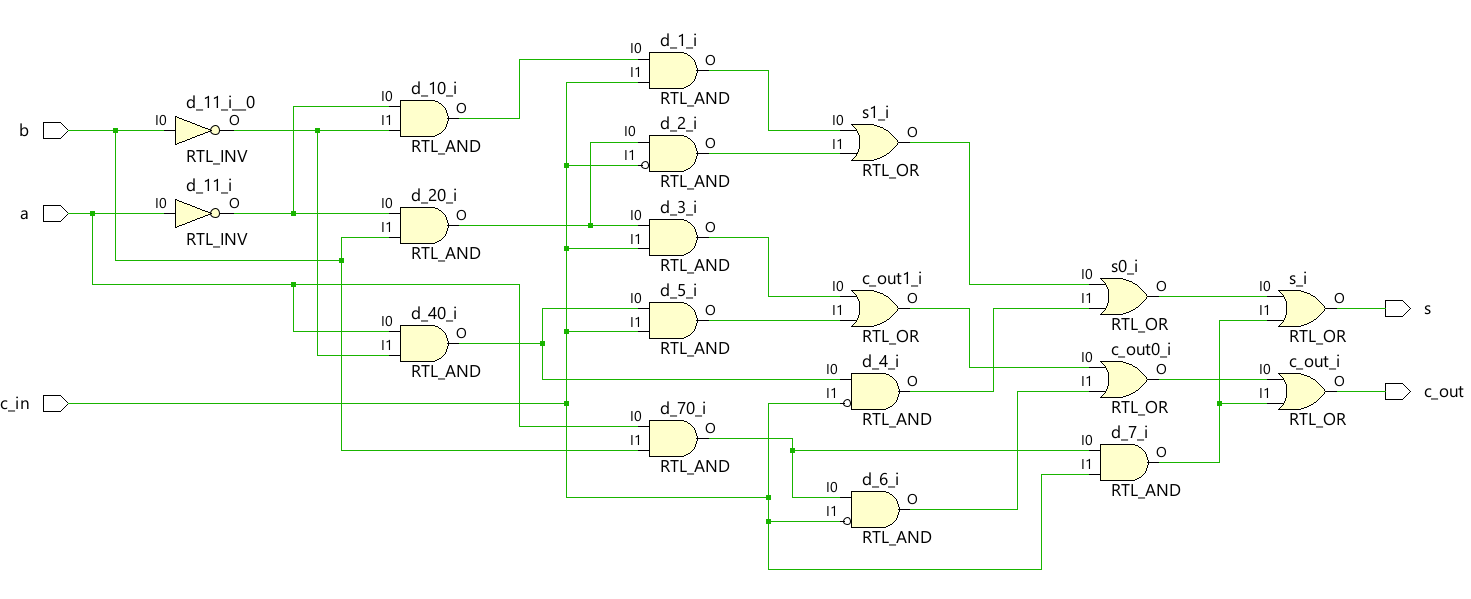
1. **Binary Multiplier**

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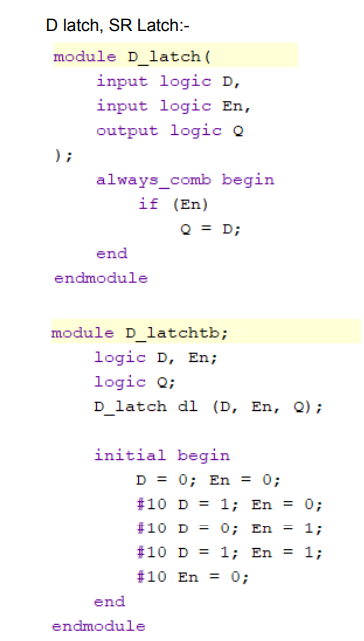
****

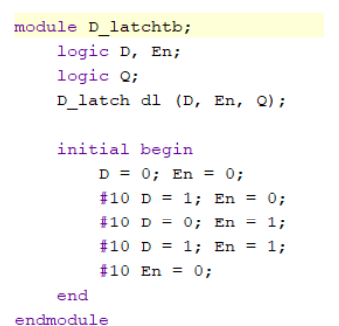
1. **Full Adder with 3 to 8 Decoder**

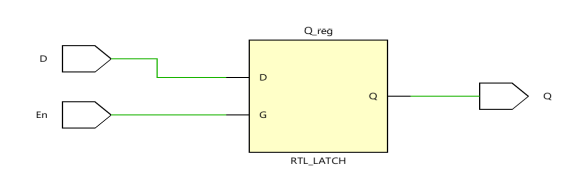
****

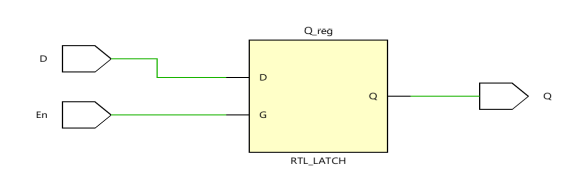
****

**21) D - Latch**

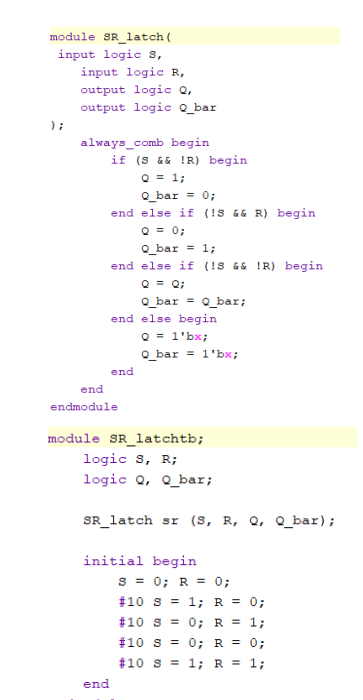
****

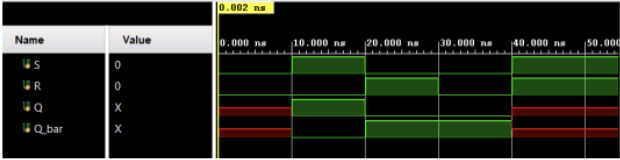
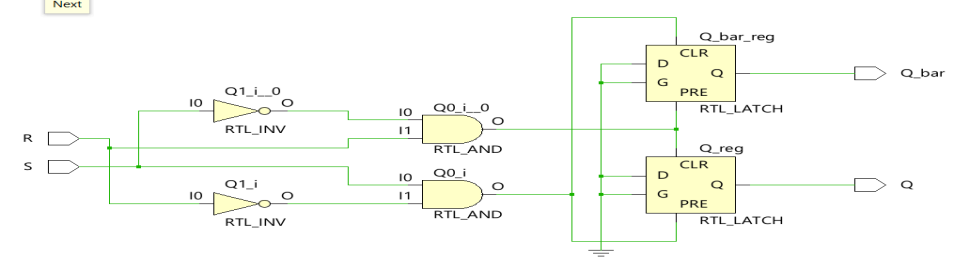
****

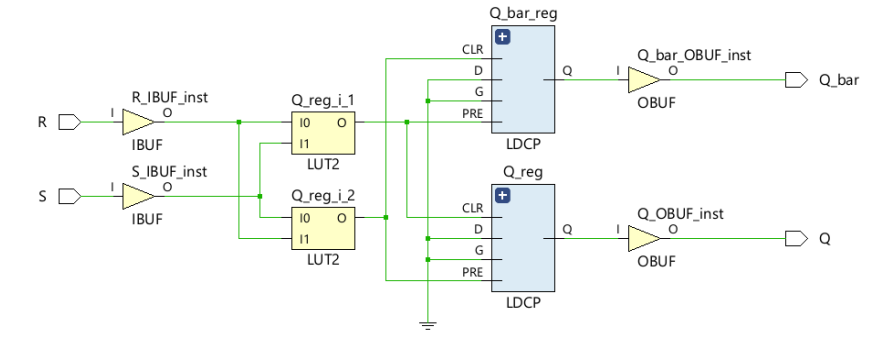
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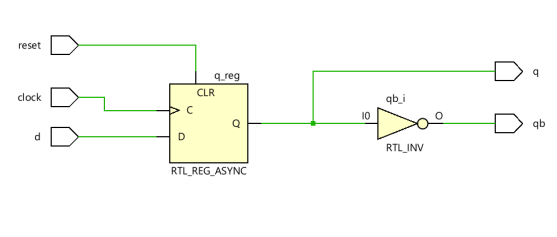
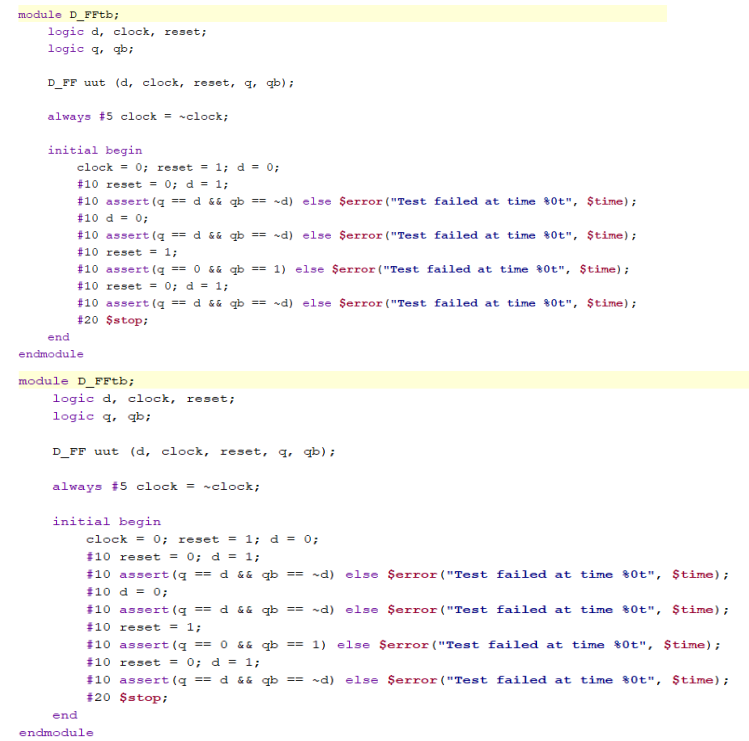
**22) SR - Latch**

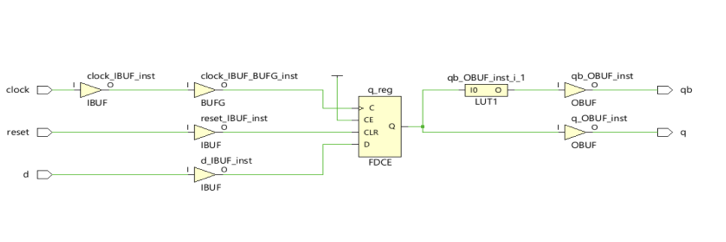
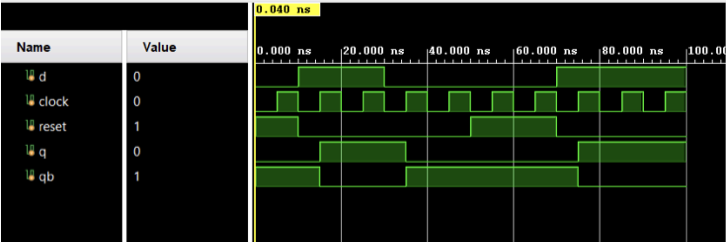
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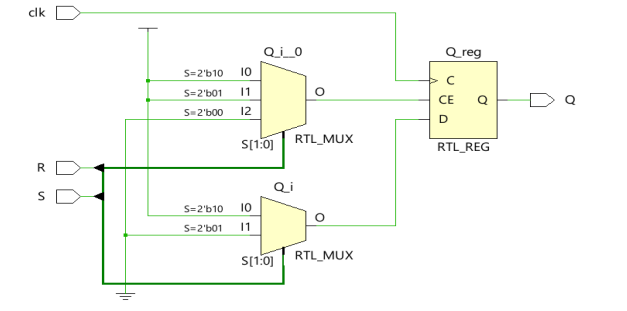
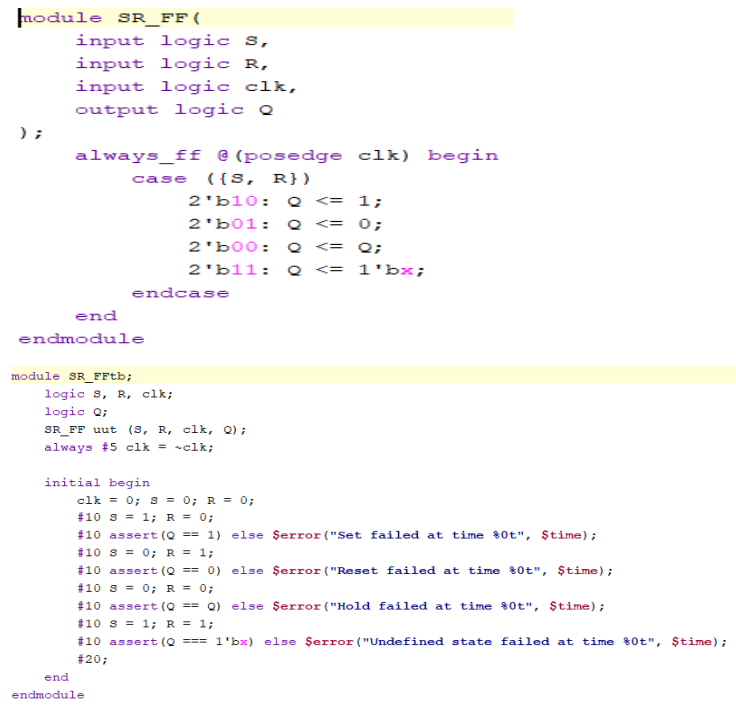
****

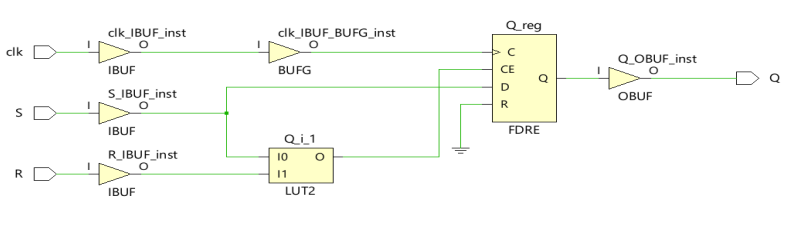
**23) D - FF**

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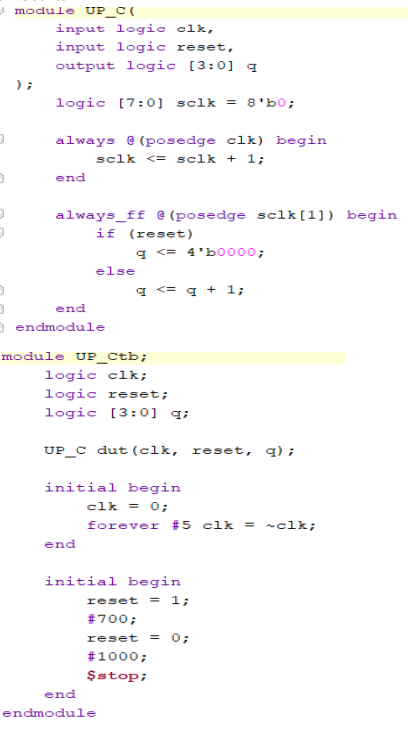
****

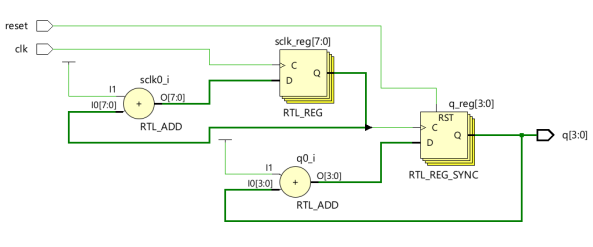
**24) SR - FF**

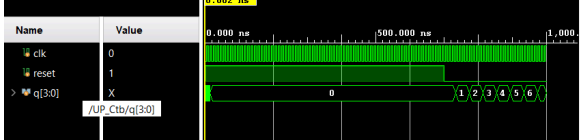
****

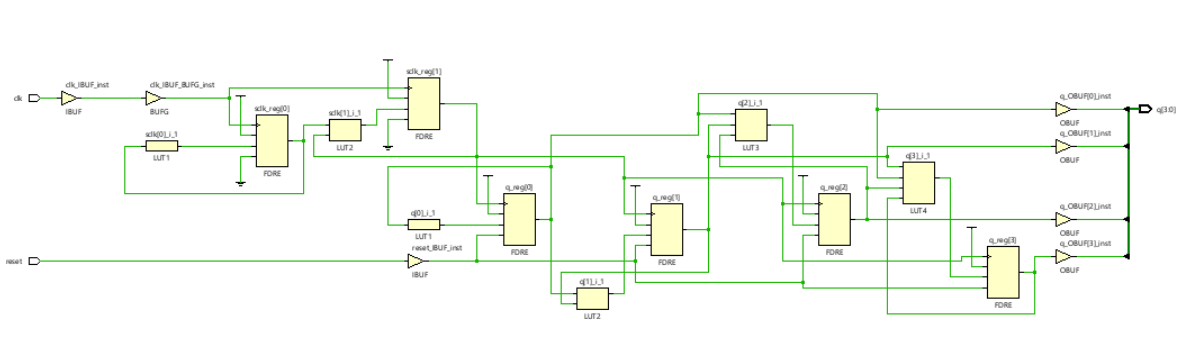
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**25) UP - Counter**

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